UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,363	07/12/2000	John M. Airey	2839/115	2211

2101 7590 07/13/2007
BROMBERG & SUNSTEIN LLP
125 SUMMER STREET
BOSTON, MA 02110-1618

EXAMINER	
WANG, JIN CHENG	
ART UNIT	PAPER NUMBER
2628	
MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/614,363	AIREY ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/18/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-13,22,26-33,35-37,45,47-56,58-60,62 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-13,22,26-33,35-37,45,47-56,58-60,62 and 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on 6/18/2007 have been entered. Claims 2, 4, 14-21, 23-25, 34, 38-44, 46, 57 and 61 have been canceled. Claims 1, 22, 45, 47-56, 58, and 62-63 have been amended. Claims 1, 3, 5-13, 22, 26-33, 35-37, 45, 47-56, 58-60, and 62-63 are pending in the application.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

2. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this

application, and all other rejections have been overcome. See 37 CFR 1.130(b).

3. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 or claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The elements of the present application's claim 1 is obvious over the elements of the patented claim 1 or the claim 25. Specifically, the patented claim 1 recites all the limitation set forth in present applicant's claim 1 or claim 25. The patented claim 1 set forth a limitation of "a rasteriziation circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format; wherein the rasterization process circuit performs scan conversion on vertices having floating point color values" which corresponds to the "a rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format" in the present application's claim 1. The patented claim 1 set forth a limitation of "the rasterization circuit performs scan conversion on vertices having floating point color values and a frame buffer coupled to the rasterization circuit for storing a plurality of color values" which corresponds to the "a frame buffer coupled to the rasterization circuit for storing a plurality of color values in the floating point format" in the present application's claim 1. The present application's claim 1 is also obvious over the patented claim 25 for the reason that a rasterization process corresponds to a scan conversion process of the claim 1 in the present application. This

is because applicant's rasterization circuit is also a scan conversion circuit. It is noted that a rasterization process performs scan conversion thereby converting the transformed primitives into pixels and a rasterization rendering is based on a scan-conversion of primitives (e.g., polygons, lines, and points). Data values generated during the scan-conversion (e.g., fragments) are blended into a frame buffer of the graphics hardware.

5. Claims 5-6 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The patented claim 25 set forth a limitation of "the the s10e5 color values stored in the frame buffer" which corresponds to the "the floating point format is comprised of sixteen bits" in the present application's claims 5-6.

6. Claims 7-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 27-31 of U.S. Pat. No. 6,650,327. The claims 7-11 further recite the claim limitations set forth in the patented claims 27-31 respectively.

7. Claim 31 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The present application's claim 31 is obvious over the patented claim 25. Specifically, the patented claim 25 recites all the limitation set forth in present applicant's claim 31. The patented claim 25 set forth a limitation of "a rasterization circuit" which is a raster subsystem for performing a rasterization process. The patented claim 25's frame buffer is a

floating point frame buffer for storing a plurality of floating point color values.

8. Claim 45 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 or claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The present application's claim 45 is obvious over the patented claim 1 or claim 25. Specifically, the patented claim 1 recites all the limitation set forth in present applicant's claim 45. The patented claim 1 set forth a limitation of "a rasteriziation circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format; wherein the rasterization process circuit performs scan conversion on vertices having floating point color values" which corresponds to the "a rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format" in the present application's claim 45. The patented claim 1 set forth a limitation of "the rasterization circuit performs scan conversion on vertices having floating point color values and a frame buffer coupled to the rasterization circuit for storing a plurality of color values" which corresponds to the "a frame buffer coupled to the rasterization circuit for storing a plurality of color values in the floating point format" in the present application's claim 45. The patent claim 1 set forth a processor, a rasterization circuit, a frame buffer which constitutes a rendering pipeline. The present application's claim 45 is also obvious over the patented claim 25 for the reason that a rasterization process corresponds to a scan conversion process of the claim 45 in the present application.

9. Claims 48-49 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The patented claim 25 set forth a limitation of "the the s10e5 color values stored in the frame buffer" which corresponds to the "the floating point format is comprised of sixteen bits" in the present application's claims 48-49.

10. Claims 50-54 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 27-31 of U.S. Pat. No. 6,650,327. The claims 50-54 further recite the claim limitations set forth in the patented claims 27-31 respectively.

11. Claim 58 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 or claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The patented claim 25 set forth a limitation of "a display screen coupled to the frame buffer for displaying an image according to the s10e5 color values stored in the frame buffer" which corresponds to "a display screen coupled to the frame buffer for receiving the plurality of color values read out from the frame buffer in the floating point format and displaying an image according to the plurality of color values" in the present application's claim 58.

12. Claim 60 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The present application's claim 60 is also obvious over the

patented claim 25 for the reason that a rasterization process corresponds to a scan conversion process of the claim 60 in the present application.

13. Claim 62 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 25 of U.S. Pat. No. 6,650,327. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason: The patented claim 25 set forth a limitation of "a display screen coupled to the frame buffer for displaying an image according to the s10e5 color values stored in the frame buffer" which corresponds to "a display screen coupled to the frame buffer for receiving the plurality of color values read out from the frame buffer in the floating point format and displaying an image according to the plurality of color values" in the present application's claim 62.

Response to Arguments

Applicant's arguments filed June 18, 2007 have been fully considered but are not found persuasive in view of the ground(s) of rejection based on **Deering U.S. Patent No. 6,115,047 (hereinafter Deering)** in view of Grossman U.S. Patent No. 5,307,450 (hereinafter Grossman) and Baum et al U.S. Patent No. 6,567,083 (hereinafter Baum).

In col. 13, lines 42-56 wherein Deering discloses the scan conversion functions/processes including edge walking and span filling wherein the steps are performed using s1.30 format 510 in Fig. 9B wherein the scan conversion process operates the fixed-point Z-values using the floating point Z-values wherein the floating point Z-values split into the common exponent portion stored in the Z exponent field. Deering also pointed out that in alternate embodiments,

different operations than those presently shown may be performed including the operations using the floating point formats in Fig. 9A and 9C. Column 7, lines 15-41 wherein "the same data" refers to the floating point data passed from the floating point processors to the drawing processors which perform the rasterization process and also the scan conversion process for converting the primitives/triangles into pixels or the screen-space representations; see also col. 3. lines 1-19; see column 9, lines 51-67 and column 10, lines 1-36 wherein the scan conversion process includes the operations set forth in the edge walker logic 322 and span fill unit 324. The edge walker logic converts polygons and rectangles to horizontal spans and the span fill unit performs an interpolation of values across oriented spans for triangles and lines. For optimized primitives including triangle span pairs, rectangle and polygon spans and antialiased lines and dots, two pixels are generated per cycle and all other primitives generate one pixel per cycle. Deering at least teaches the scan conversion process operates the triangles, primitives or polygons using the Z-values of the primitives, triangles and/or polygons in the floating point format wherein the z-values are output from the floating point processors.

Deering discloses in column 11-12, especially column 12, lines 20-30, operates the Z-values wherein each Z-value has a mantissa portion and an exponent portion. Since the it is statistically likely that all vertices of a given primitive will have the same exponent for all Z-values and the floating point Z-values are broken up into the common exponent portion and the fixed point z-values wherein it is efficient or sufficient to perform some operations based on the fixed point portions of the Z-values or the transformed Z-values; see column 13 wherein the scan conversion process operates using the floating point Z-values and some scan conversion operations are performed using the floating point Z-values including calculating the fixed point

portions of the Z-values because all vertices of a given primitive have the common exponent portion of the floating-point Z-values; see column 16, lines 4-40. In view of the claim limitation of "scan conversion process", Deering teaches edge walking and scan interpolation within the drawing processors. In accordance with Deering-682, the drawing processors perform the scan conversion process. This is because Deering-682 discloses column 5, lines 63-67 that the scan conversion functions include edgewalking function and scan interpolation and thus Deering's drawing processors perform the scan conversion process of edgewalking function and scan interpolation function based on the floating values or the s1.30 values shown in Figs. 9A-9C. Deering discloses that different operations than directly calculating the s1.30 values may be performed including the operations directly using the floating point formats in Fig. 9A and 9C.

Baum discloses a floating-point frame buffer storing the floating point color image values (See Baum column 12, lines 48-64 and column 11, lines 1-42).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to have incorporated Baum's floating point frame buffer for storing the color values because Deering teaches a floating point frame buffer for storing the z-values and suggests that the same hardware may be reused for the color values (Deering column 16, lines 30-35). Deering teaches column 1, lines 25-30 that position, color such as red, blue, green are typically represented as floating point values wherein the frame buffer is 96-bit deep (See Deering column 7, lines 30-35) and therefore suggesting an obvious modification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5-13, 22, 26-33, 35-37, 45, 47-56, 58-60, and 62-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Deering U.S. Patent No. 6,115,047 (hereinafter Deering)** in view of Deering U.S. Patent No. 5,440,682 (hereinafter Deering-682) and Baum et al U.S. Patent No. 6,567,083 (hereinafter Baum).

Re claims 1 and 45, Deering teaches a processor for performing geometric calculations on a plurality of vertices of a primitive (*e.g., the floating point processors receive high level drawing commands and generate graphics primitives such as triangles, lines for rendering three-dimensional objects on the screen. The floating point processors perform transformation, clipping, face determination, lighting and set-up operations on received geometry data; see column 6, lines 55-67 wherein the set-up calculations for all primitives include computing the distances in multiple dimensions from one vertex to another and calculating slopes along that edge; see column 8, lines 24-29*);

A rasterization circuit coupled to the processor that rasterizes the primitive according to a scan conversion process which operates using a floating point format (*col. 13, lines 42-56 wherein Deering discloses the scan conversion functions/processes including edge walking and span filling wherein the steps are performed using s1.30 format 510 in Fig. 9B wherein the scan*

conversion process operates the fixed-point Z-values using the floating point Z-values wherein the floating point Z-values split into the common exponent portion stored in the Z exponent field. Deering also pointed out that in alternate embodiments, different operations than those presently shown may be performed including the operations using the floating point formats in Fig. 9A and 9C. Column 7, lines 15-41 wherein "the same data" refers to the floating point data passed from the floating point processors to the drawing processors which perform the rasterization process and also the scan conversion process for converting the primitives/triangles into pixels or the screen-space representations; see also col. 3. lines 1-19; see column 9, lines 51-67 and column 10, lines 1-36 wherein the scan conversion process includes the operations set forth in the edge walker logic 322 and span fill unit 324. The edge walker logic converts polygons and rectangles to horizontal spans and the span fill unit performs an interpolation of values across oriented spans for triangles and lines. For optimized primitives including triangle span pairs, rectangle and polygon spans and antialiased lines and dots, two pixels are generated per cycle and all other primitives generate one pixel per cycle. Deering at least teaches the scan conversion process operates the triangles, primitives or polygons using the Z-values of the primitives, triangles and/or polygons in the floating point format wherein the z-values are output from the floating point processors. Deering discloses in column 11-12, especially column 12, lines 20-30, operates the Z-values wherein each Z-value has a mantissa portion and an exponent portion. Since the it is statistically likely that all vertices of a given primitive will have the same exponent for all Z-values and the floating point Z-values are broken up into the common exponent portion and the fixed point z-values wherein it is efficient or sufficient to perform some operations based on the fixed point portions of the Z-values or the transformed Z-values; see column 13 wherein

the scan conversion process operates using the floating point Z-values and some scan conversion operations are performed using the floating point Z-values including calculating the fixed point portions of the Z-values because all vertices of a given primitive have the common exponent portion of the Z-values; see column 16, lines 4-40. In view of the claim limitation of "scan conversion process", Deering teaches edge walking and scan interpolation within the drawing processors. In accordance with Deering-682, the drawing processors perform the scan conversion process. This is because Deering-682 discloses column 5, lines 63-67 that the scan conversion functions include edgewalking function and scan interpolation and thus Deering's drawing processors perform the scan conversion process of edgewalking function and scan interpolation function based on the floating values or the s1.30 values shown in Figs. 9A-9C),

A frame buffer coupled to the rasterization circuit for storing a plurality of color values in floating point formats (***col. 7, lines 30-35 wherein Deering's frame buffer is 96-bit deep and col. 16, lines 20-30 wherein Deering teaches that a floating point Z-value is conveyed and the value is conveyed to frame buffer interface 336 and on to frame buffer 100 and therefore, Deering's frame buffer is a floating point frame buffer storing a plurality of depth values in floating point formats. Deering also discloses in column 16, lines 30-35 that the same hardware that processes color and alpha values within the graphics pipeline may be reused.*** *Column 2, lines 12-41. col. 3. lines 20-32 and column 16, lines 4-40 wherein the floating point Z-value is conveyed to frame buffer interface 336 and on to frame buffer 100*).

In other words, Deering teaches a floating point frame buffer such as the frame buffer 100 for storing floating point z-values (See Deering **column 14, lines 15-25 wherein the Z-values resulting from the fixed-to-float conversion process are then used to perform hidden**

surface removal operations within frame buffer 100 and column 16, lines 16-30) and "a display screen coupled to the frame buffer for receiving the plurality of image values read out from the frame buffer in the floating point format wherein Deering teaches rendering the floating-point z-values from the floating point frame buffer 100 (See Deering column 14, lines 15-20 and **column 17, lines 10-20**) and Deering teaches that the floating point z-values representing z coordinates for vertices of triangle primitives usable **to render** three-dimensional objects on display device 84 (column 10, lines 60-67 and column 11, lines 1-5).

Deering additionally discloses the claim limitation of a processor for performing geometric calculations on a plurality of vertices of a primitive wherein Deering teaches the floating point processors 152A-152F of Fig. 6 including the F-core block 202 for performing the floating point intensive operations (which performs fixed point calculations as well) including the geometry transformation, clip testing, face determination, perspective division and screen space conversion (See column 7, lines 50-67).

Deering additionally discloses the claim limitation of a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates using a floating point format wherein Deering teaches the draw processor 172A and 172B rasterizes the primitive (See column 9, lines 50-67 and column 10, lines 1-50) wherein the rasterization process or the scan conversion process includes partitioning primitives into pieces, sending a line description to the span field unit, performing an interpolation of values across arbitrarily oriented spans for triangles and lines, performing blending, anti-aliasing, depth cueing and setup for logical operations, etc. See Deering column 9, lines 50-67 and column 10, lines 1-50. The drawing processors 172A and 172B outputs floating-point z-values to the floating point frame

buffer 100 (See **column 14, lines 13-24**). Therefore, Deering's draw processor includes the scan conversion process operates Z-values using Z-values in a floating point format.

In col. 13, lines 42-56 wherein Deering discloses the scan conversion functions/processes including edge walking and span filling wherein the steps are performed using s1.30 format 510 in Fig. 9B wherein the scan conversion process operates the fixed-point Z-values using the floating point Z-values wherein the floating point Z-values split into the common exponent portion stored in the Z exponent field. Deering also pointed out that in alternate embodiments, different operations than those presently shown may be performed including the operations using the floating point formats in Fig. 9A and 9C. Column 7, lines 15-41 wherein "the same data" refers to the floating point data passed from the floating point processors to the drawing processors which perform the rasterization process and also the scan conversion process for converting the primitives/triangles into pixels or the screen-space representations; see also col. 3. lines 1-19; see column 9, lines 51-67 and column 10, lines 1-36 wherein the scan conversion process includes the operations set forth in the edge walker logic 322 and span fill unit 324. The edge walker logic converts polygons and rectangles to horizontal spans and the span fill unit performs an interpolation of values across oriented spans for triangles and lines. For optimized primitives including triangle span pairs, rectangle and polygon spans and antialiased lines and dots, two pixels are generated per cycle and all other primitives generate one pixel per cycle. Deering at least teaches the scan conversion process operates the triangles, primitives or polygons using the Z-values of the primitives, triangles and/or polygons in the floating point format wherein the z-values are output from the floating point processors.

Deering discloses in column 11-12, especially column 12, lines 20-30, operates the Z-values wherein each Z-value has a mantissa portion and an exponent portion. Since the it is statistically likely that all vertices of a given primitive will have the same exponent for all Z-values and the floating point Z-values are broken up into the common exponent portion and the fixed point z-values wherein it is efficient or sufficient to perform some operations based on the fixed point portions of the Z-values or the transformed Z-values; see column 13 wherein the scan conversion process operates using the floating point Z-values and some scan conversion operations are performed using the floating point Z-values including calculating the fixed point portions of the Z-values because all vertices of a given primitive have the common exponent portion of the floating-point Z-values; see column 16, lines 4-40. In view of the claim limitation of "scan conversion process", Deering teaches edge walking and scan interpolation within the drawing processors. In accordance with Deering-682, the drawing processors perform the scan conversion process. This is because Deering-682 discloses column 5, lines 63-67 that the scan conversion functions include edgewalking function and scan interpolation and thus Deering's drawing processors perform the scan conversion process of edgewalking function and scan interpolation function based on the floating values or the s1.30 values shown in Figs. 9A-9C. Deering discloses that different operations than directly calculating the s1.30 values may be performed including the operations directly using the floating point formats in Fig. 9A and 9C.

It is OLD and well known in a scan-conversion process to operate using floating-point format as Grossman demonstrates back in 1994. Grossmann discloses a scan-conversion method scan-converting primitives that requires the floating point arithmetic (Grossman column 5-6 wherein the scan conversion subsystem includes the Vertex Reorganizer, the Polygon Engine

and the Area Engine and the Span Processor and the floating point precision is used in the stages up to and including the Poly Engine).

Therefore, having the combined teaching of Deering and Grossman as a whole, one of ordinary skill in the art would have found it obvious to perform a scan conversion which operates using the floating point format (**Deering column 4, lines 25-30** and Kaufman Page 62).

Although Deering discloses a floating point frame buffer storing the floating point z-values, Deering is silent to a frame buffer storing color values in the floating point formats.

Baum discloses a floating point frame buffer storing the floating point color image values (See Baum column 12, lines 58-64).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to have incorporated Baum's floating point frame buffer for storing the color values because Deering teaches a floating point frame buffer for storing the z-values and suggests that the same hardware may be reused for the color values (Deering column 16, lines 30-35). Deering teaches column 1, lines 25-30 that position, color such as red, blue, green are typically represented as floating point values wherein the frame buffer is 96-bit deep (See Deering column 7, lines 30-35) and therefore suggesting an obvious modification.

Therefore, having the combined teaching of Deering and Kaufman and Baum as a whole, one of ordinary skill in the art would have found it obvious to perform a scan conversion which operates using the floating point format (**Deering column 4, lines 25-30**).

Re claims 3 and 47, Deering discloses a texture circuit coupled to the rasterization circuit with the graphics pipeline that applies a texture to the primitive, wherein the texture is specified

by floating point values and a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values (See Deering column 10, lines 20-50).

Re claims 5 and 48, Deering discloses the floating-point format is comprised of sixteen bits (Deering Fig. 9A and 9C).

Deering discloses floating-point values have 16 bits (Deering Figs. 9A and 9C)

Re claims 7 and 50, Deering discloses a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on floating point values (**Deering column 7, lines 50-67 and column 8, lines 1-23**).

Re claims 6, 8-13 and 22, 49, and 51-56, 58-60 and 62-63, the limitations of claims 6, 8-13, 22, 49 and 51-56, 58-60 and 62-63 are analyzed as discussed with respect to claim 1.

Re claim 26, Deering discloses the steps of writing, storing, and reading the data in the frame buffer in the floating point format are further comprised of specifying the floating-point format according to a specification, wherein the specification corresponds to a level of range and precision (**Deering Fig 9 and column 14, lines 13-23**).

Re claim 31, Deering discloses a computer system comprising a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format and a floating point frame buffer coupled to the raster subsystem for storing a plurality of floating point color values (Deering Figs. 3-7). In other words, Deering teaches a typical computer graphics system include a raster subsystem in a graphics pipeline.

The output from the geometry accelerator, referred to as rendering data, is used by the rasterizer (and optional texture mapping hardware) to compute final screen space coordinates and

R, G, B color values for each pixel constituting the primitives. The pixel data is stored in the frame buffer for display on a display screen. In that the geometry accelerator may be required to perform on the order of hundreds of millions of floating point calculations per second per chip. Functions of the geometry accelerator may include three-dimensional transformation, lighting, clipping, and perspective divide operations as well as plane equation generation, performed in floating point format. Geometry accelerator functions result in rendering data which is sent to the frame buffer subsystem for rasterization.

Deering teaches a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format. Deering teaches the draw processor 172A and 172B rasterizes the primitive (See column 9, lines 50-67 and column 10, lines 1-50) wherein the rasterization process includes partitioning primitives into pieces, sending a line description to the span field unit, performing an interpolation of values across arbitrarily oriented spans for triangles and lines, performing blending, anti-aliasing, depth cueing and setup for logical operations, etc. See Deering column 9, lines 50-67 and column 10, lines 1-50. The drawing processors 172A and 172B outputs floating point z-values to the floating point frame buffer 100 (See **column 14, lines 13-24**). Therefore, Deering's draw processor operates using a floating point format.

Deering additionally discloses a processor for performing geometric calculations on a plurality of vertices of a primitive wherein Deering teaches the floating point processors 152A-152F of Fig. 6 including the F-core block 202 for performing the floating point intensive operations (which performs fixed point calculations as well) including the geometry transformation, clip testing, face determination, perspective division and screen space conversion

(See column 7, lines 50-67). The floating point processors 152A-152F also rasterizes the primitive according to a rasterization process which operates using a floating point format.

Deering discloses a floating point frame buffer coupled to the raster subsystem for storing a plurality of floating point color values, wherein the floating point color values are read out from the frame buffer in the floating point format for display. Deering teaches a floating point frame buffer such as the frame buffer 100 for storing floating point z-values (See Deering **column 14, lines 15-20** and column 16, lines 16-30). Deering teaches rendering the floating-point z-values from the floating point frame buffer 100 (See Deering column 14, lines 15-20 and **column 17, lines 10-20**) and Deering teaches that the floating point z-values representing z coordinates for vertices of triangle primitives usable **to render** three-dimensional objects on display device 84 (column 10, lines 60-67 and column 11, lines 1-5).

Re claims 32-33 and 35, Deering discloses the floating point color values are written to, read from (for display purposes), and stored in the frame buffer (**Deering column 10, lines 60-67 and column 11, lines 1-5**).

Re claims 36-37, Deering discloses the floating point color values are comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits (Deering Fig. 9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw Jinchengwang